ABSTRACT OF THE DISCLOSURE

This invention provides a nonvolatile semiconductor memory device including a novel memory core portion in which an influence of a parasitic element component in a memory cell information reading path is excluded in a reading operation, and novel sensing means accompanying this memory core structure, so as to achieve rapid sensing. In the memory core portion, a selected memory cell is selected by a global bit line through a local bit line and an adjacent global bit line is connected to a local bit line in a non-selected sector. A column selecting portion connects a pair of the global bit lines to a pair of data bus lines. A load portion having a load equivalent to a parasitic capacitance of a path leading from the memory cell and for supplying a reference current to a reference side is connected to a pair of the data bus lines. A current of the memory cell information is compared with the reference current by a current comparing portion and a differential current is outputted. A path load is equalized by a pair of adjacent paths so that an effect from noise is canceled, thus making it possible to achieve rapid reading.